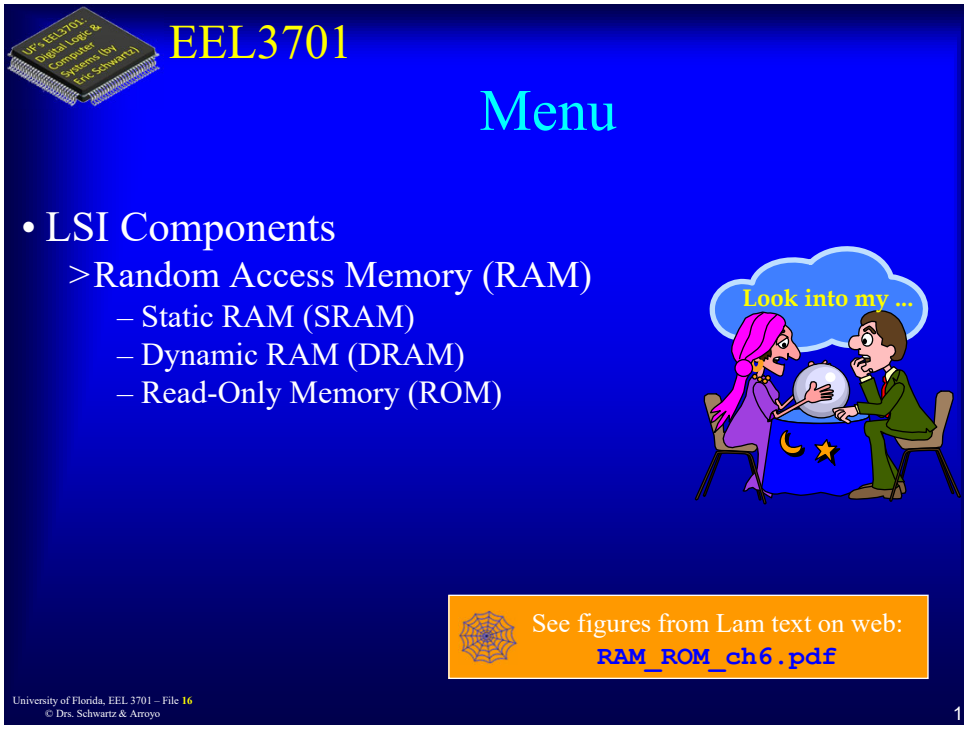
EEL3701
Menu
• LSI Components
>Random Access Memory (RAM)
– Static RAM (SRAM)
– Dynamic RAM (DRAM)
– Read-Only Memory (ROM)
Look into my ...
See figures from Lam text on web:
RAM_ROM_ch6.pdf
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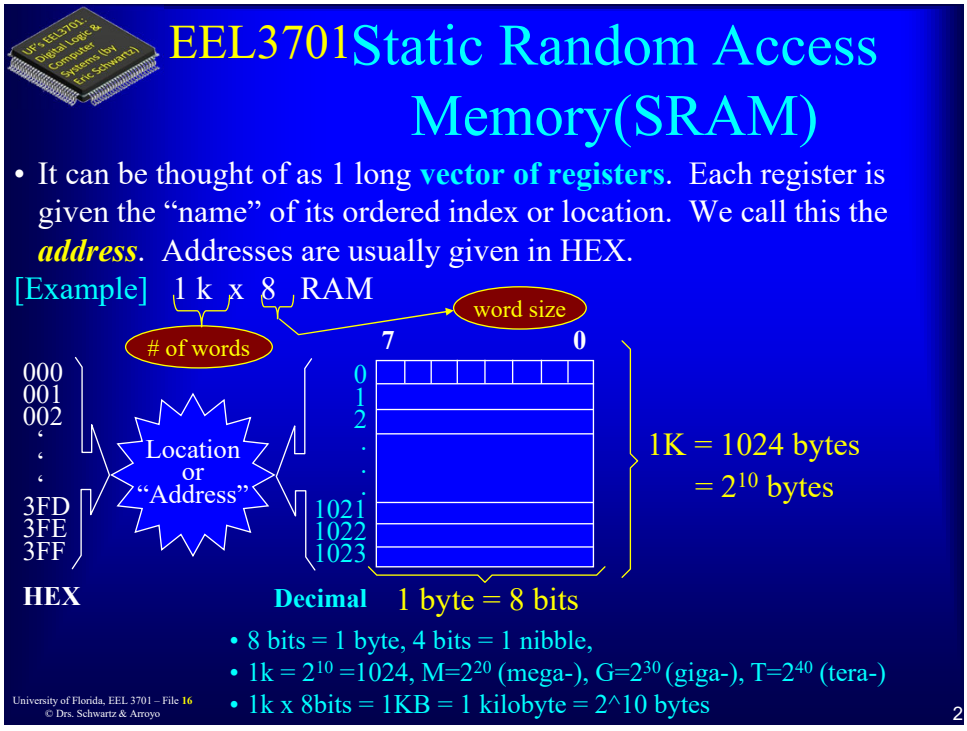
1

1


EEL3701 Static Random Access Memory(SRAM)
• It can be thought of as 1 long vector of registers. Each register is given the "name" of its ordered index or location. We call this the address. Addresses are usually given in HEX.
[Example] 1 k x 8 RAM
word size
# of words
7
0
000
001
002
3FD
3FE
3FF
Location or "Address"
0
1
2
1021
1022
1023
1K = 1024 bytes
= 2^10 bytes
HEX
Decimal
1 byte = 8 bits
• 8 bits = 1 byte, 4 bits = 1 nibble,
• 1k = 2^10 =1024, M=2^20 (mega-), G=2^30 (giga-), T=2^40 (tera-)
• 1k x 8bits = 1KB = 1 kilobyte = 2^10 bytes
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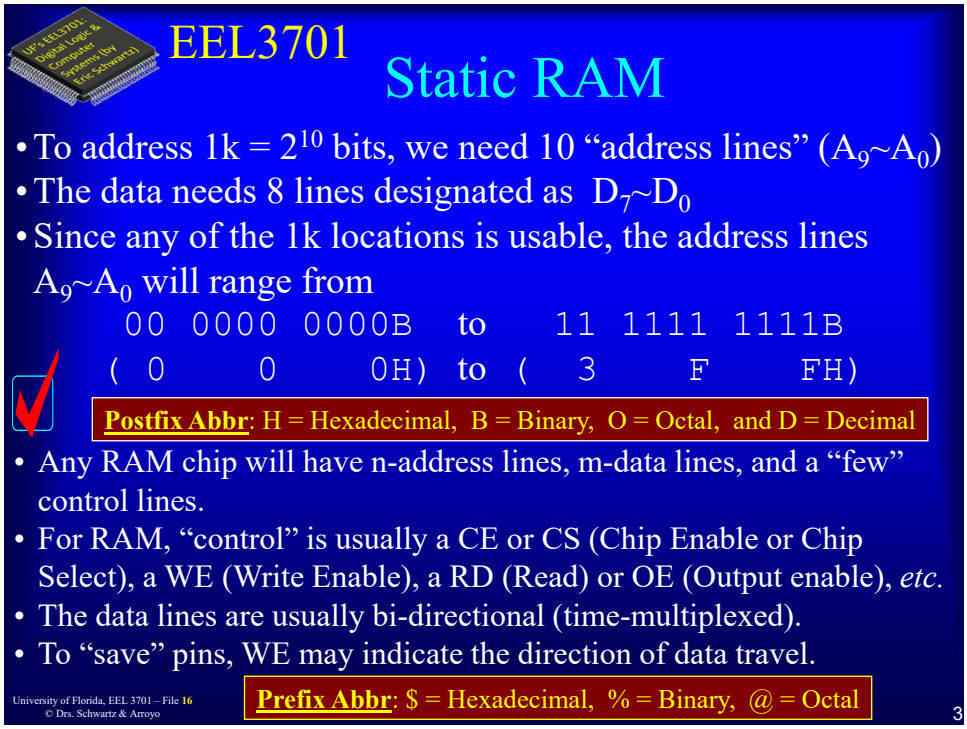
2

2


EEL3701
Static RAM
• To address 1k = 2^10 bits, we need 10 "address lines" (A9~A0)
• The data needs 8 lines designated as D7~D0
• Since any of the 1k locations is usable, the address lines A9~A0 will range from
00 0000 0000B to 11 1111 1111B
(0 0 0H) to (3 F FH)
Postfix Abbr: H = Hexadecimal, B = Binary, O = Octal, and D = Decimal
• Any RAM chip will have n-address lines, m-data lines, and a "few" control lines.
• For RAM, "control" is usually a CE or CS (Chip Enable or Chip Select), a WE (Write Enable), a RD (Read) or OE (Output enable), etc.
• The data lines are usually bi-directional (time-multiplexed).
• To "save" pins, WE may indicate the direction of data travel.
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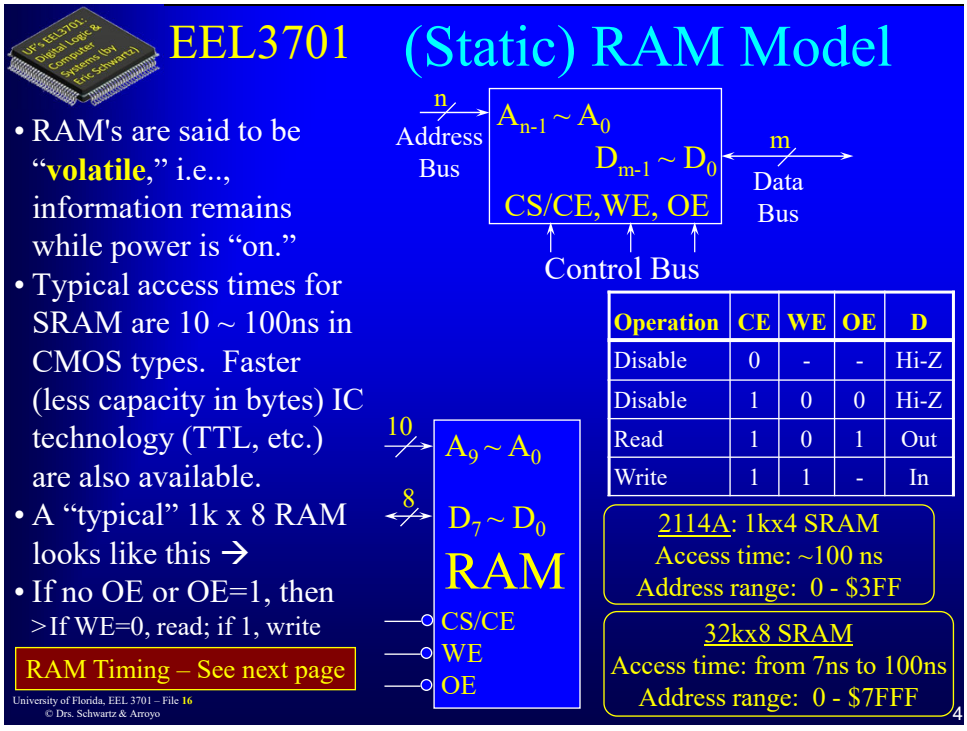
Prefix Abbr: $ = Hexadecimal, % = Binary, @ = Octal
3

3


EEL3701
(Static) RAM Model
• RAM's are said to be "volatile," i.e.., information remains while power is "on."
• Typical access times for SRAM are 10 ~ 100ns in CMOS types. Faster (less capacity in bytes) IC technology (TTL, etc.) are also available.
• A "typical" 1k x 8 RAM looks like this →
• If no OE or OE=1, then
>If WE=0, read; if 1, write
RAM Timing – See next page
n
Address Bus
An-1 ~ A0
Dm-1 ~ D0
CS/CE,WE, OE
m
Data Bus
Control Bus
10
A9 ~ A0
8
D7 ~ D0
RAM
CS/CE
WE
OE
Operation CE WE OE D
Disable 0 - - Hi-Z
Disable 1 0 0 Hi-Z
Read 1 0 1 Out
Write 1 1 - In
2114A: 1kx4 SRAM
Access time: ~100 ns
Address range: 0 - $3FF
32kx8 SRAM
Access time: from 7ns to 100ns
Address range: 0 - $7FFF
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4

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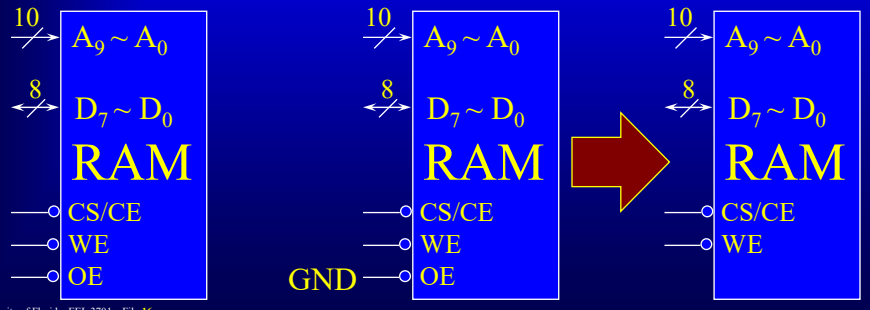
Simplified SRAM

- Sometimes block diagrams for SRAM are simplified, removing OE(L).
  - >Since WE(L) has higher priority than OE(L), OE(L) can be always true, i.e., GND.
  - >In this case, if WE is true, writing to SRAM; otherwise reading.



5

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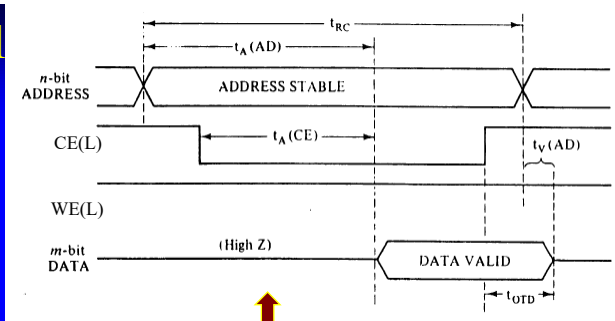
SRAM Timing Diagrams

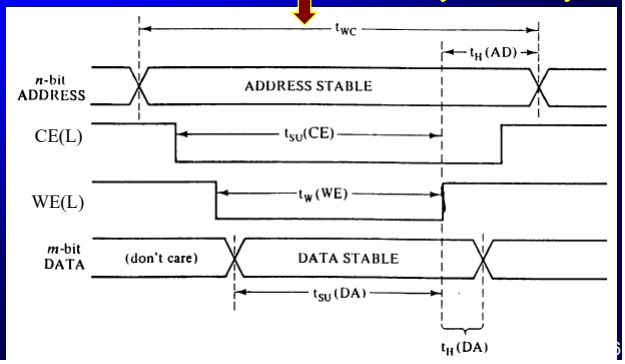
- Since no OE, the WE determines read or write cycles

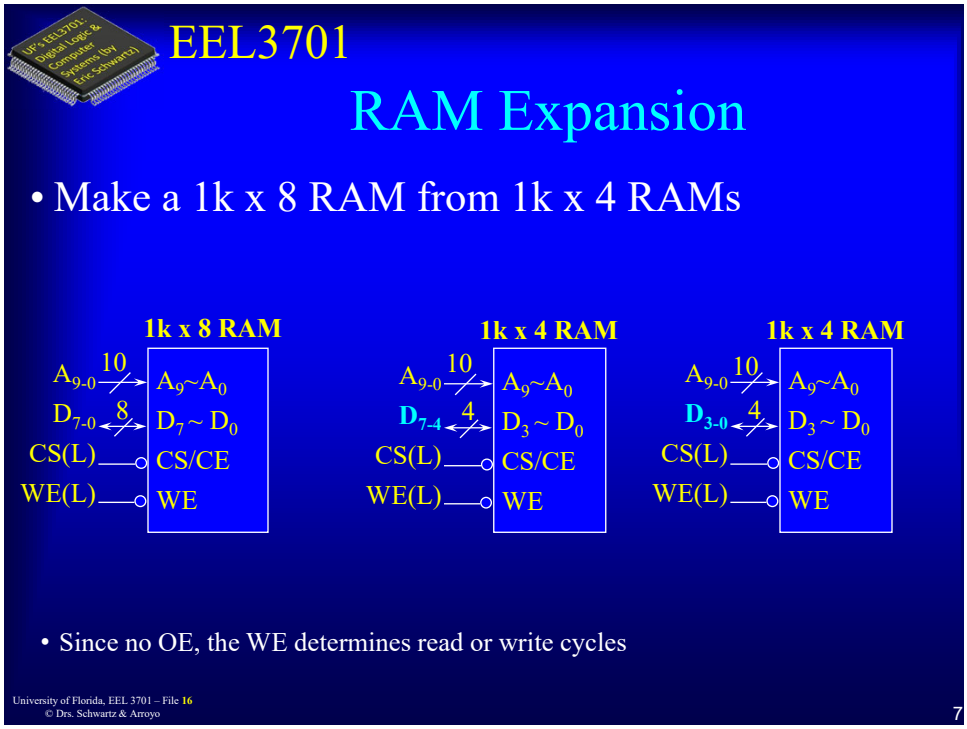
Ref: Lam Fig 6.26



Memory Read Cycle

Memory Write Cycle




EEL3701
RAM Expansion
• Make a 1k x 8 RAM from 1k x 4 RAMs
1k x 8 RAM
A9-0 10
D7-0 8
CS(L)
WE(L)
A9~A0
D7 ~ D0
CS/CE
WE
1k x 4 RAM
A9-0 10
D7-4 4
CS(L)
WE(L)
A9~A0
D3 ~ D0
CS/CE
WE
1k x 4 RAM
A9-0 10
D3-0 4
CS(L)
WE(L)
A9~A0
D3 ~ D0
CS/CE
WE
• Since no OE, the WE determines read or write cycles
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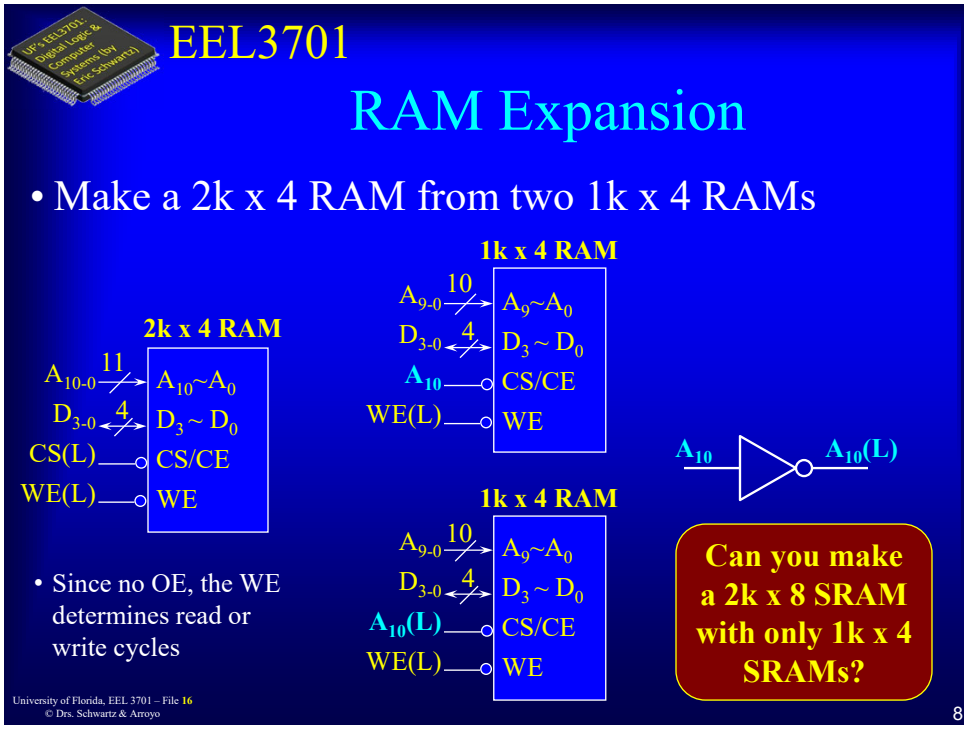
7

7


EEL3701
RAM Expansion
• Make a 2k x 4 RAM from two 1k x 4 RAMs
2k x 4 RAM
A10-0 11
D3-0 4
CS(L)
WE(L)
A10~A0
D3 ~ D0
CS/CE
WE
1k x 4 RAM
A9-0 10
D3-0 4
A10
WE(L)
A9~A0
D3 ~ D0
CS/CE
WE
1k x 4 RAM
A9-0 10
D3-0 4
A10(L)
WE(L)
A9~A0
D3 ~ D0
CS/CE
WE
A10
A10(L)
Can you make a 2k x 8 SRAM with only 1k x 4 SRAMs?
• Since no OE, the WE determines read or write cycles
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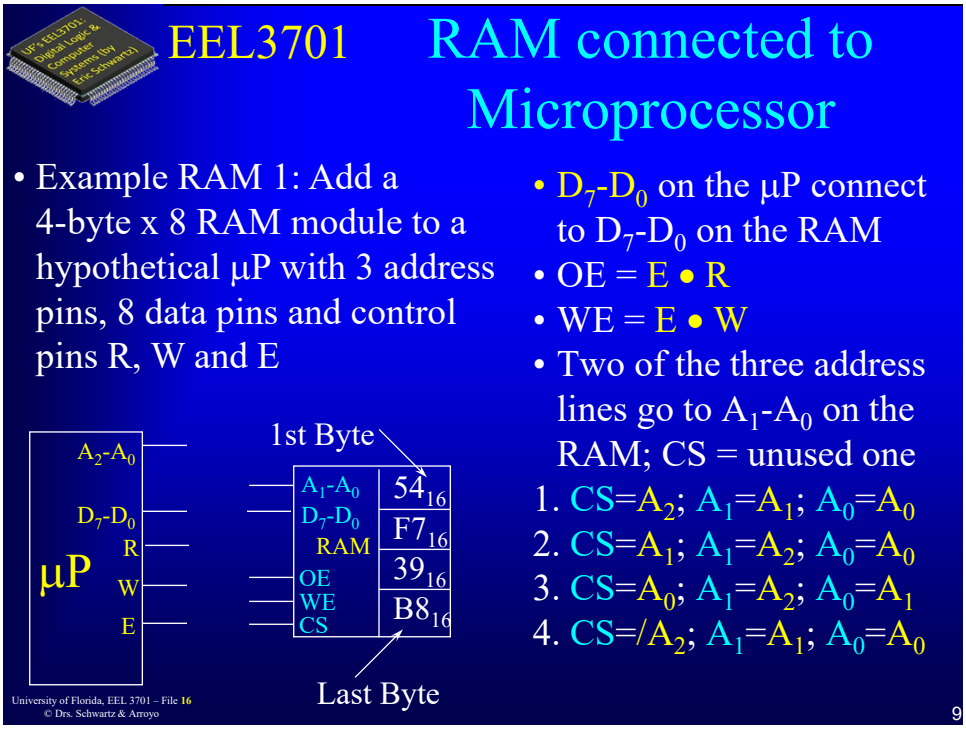
EEL3701
RAM connected to Microprocessor
• Example RAM 1: Add a 4-byte x 8 RAM module to a hypothetical µP with 3 address pins, 8 data pins and control pins R, W and E
• D_7-D_0 on the µP connect to D_7-D_0 on the RAM
• OE = E • R
• WE = E • W
• Two of the three address lines go to A_1-A_0 on the RAM; CS = unused one
1. CS=A_2; A_1=A_1; A_0=A_0
2. CS=A_1; A_1=A_2; A_0=A_0
3. CS=A_0; A_1=A_2; A_0=A_1
4. CS=/A_2; A_1=A_1; A_0=A_0
A_2-A_0
D_7-D_0
R
W
E
µP
1st Byte
A_1-A_0
D_7-D_0
RAM
OE
WE
CS
54_{16}
$F7_{16}$
39_{16}
$B8_{16}$
Last Byte
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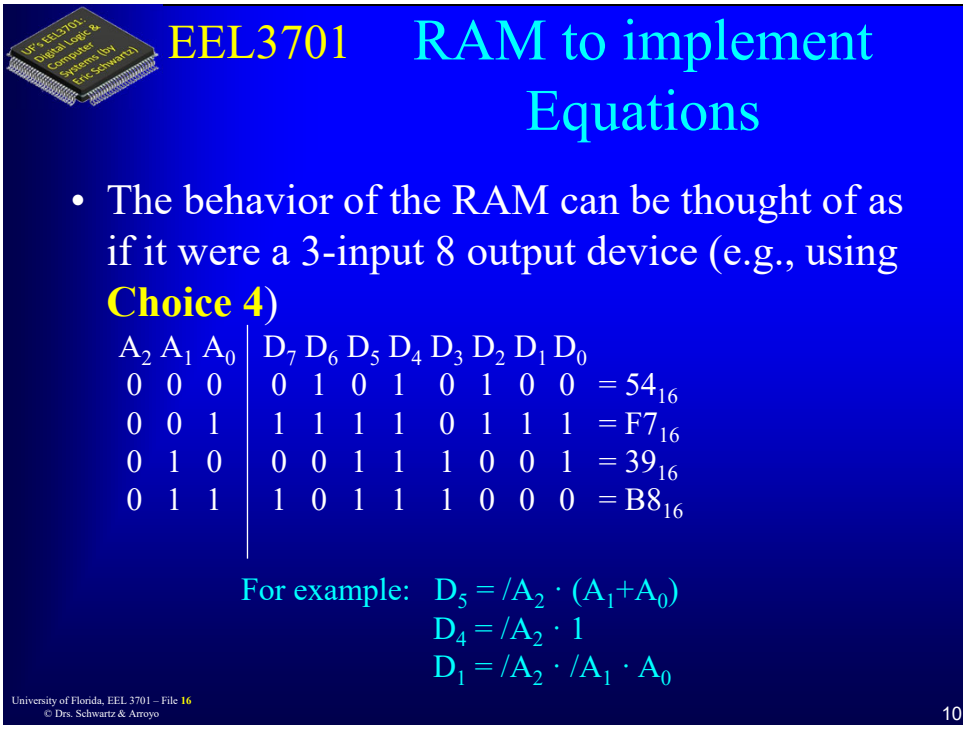
9

9


EEL3701
RAM to implement Equations
• The behavior of the RAM can be thought of as if it were a 3-input 8 output device (e.g., using **Choice 4**)
A_2 A_1 A_0 | D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
0 0 0 | 0 1 0 1 0 1 0 0 = 54_{16}
0 0 1 | 1 1 1 1 0 1 1 1 = $F7_{16}$
0 1 0 | 0 0 1 1 1 0 0 1 = 39_{16}
0 1 1 | 1 0 1 1 1 0 0 0 = $B8_{16}$
For example: D_5 = /A_2 · (A_1+A_0)
D_4 = /A_2 · 1
D_1 = /A_2 · /A_1 · A_0
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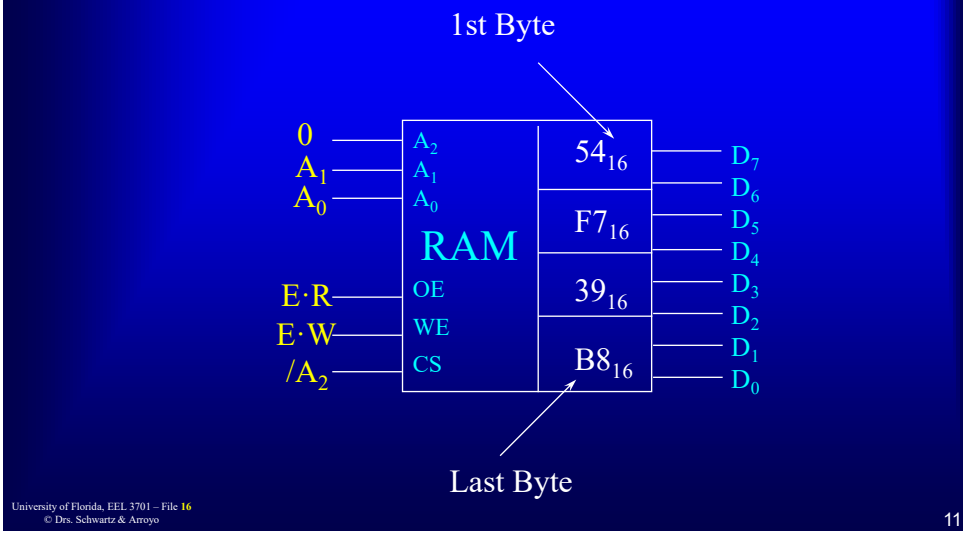
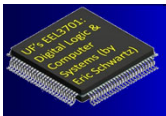
EEL3701 RAM connected to Microprocessor



EEL3701 RAM connected to µP

- What are the consequences of these choices?
  - >Choice 1: CS=A2; A1=A1; A0=A0
    - – When the mP issues address 000; the RAM does not respond since CS=A2=0; similarly for addresses 001, 010, 011
    - – For address 100 the mP reads $54, for 101 the mP reads $F7, for 110 the mP reads $39, for 111 the mP reads $B8
    - – The 4-byte RAM starts at address 100

Address	Choice 1	Choice 2	Choice 3	Choice 4
0 0 0	None	None	None	$54
0 0 1	None	None	$54	$F7
0 1 0	None	$54	None	$39
0 1 1	None	$F7	$F7	$B8
1 0 0	$54	None	None	None
1 0 1	$F7	None	$39	None
1 1 0	$39	$39	None	None
1 1 1	$B8	$B8	$F8	None



EEL3701

Conclusions from Example RAM 1

- The data in the RAM will not be accessed contiguously unless we connect the matching contiguous low order lines to the RAM ∴ A_1=A_1 and A_0=A_0
- We have a choice of CS=/A_2 or CS=A_2; if we want the RAM in the "low memory range" choose CS=/A_2; if in the "high memory range" CS=A_2
- For contiguous access we always connect the low order address pins to **all** the RAM address pins
- CS = *f* (unused high order address lines). If we have m unused address lines we will have $\mathbf{2^m}$ starting addresses for the contiguous memory block

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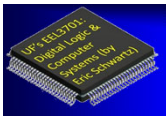
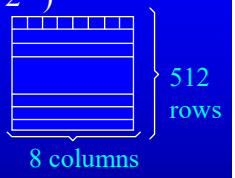


EEL3701

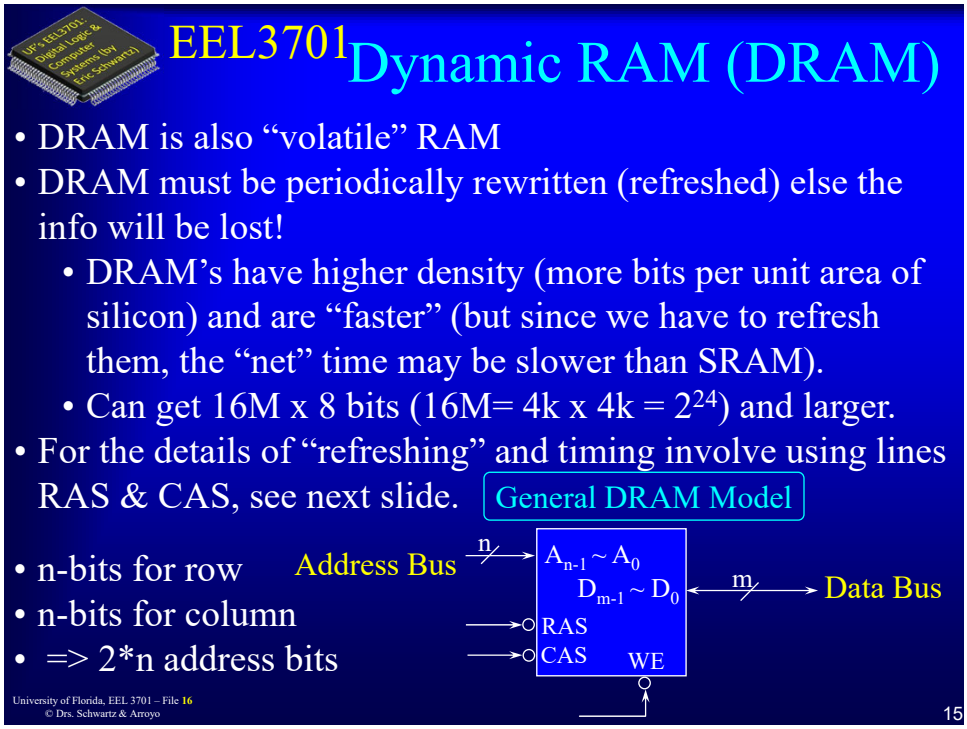
Data Arrangement in RAM

- Sometimes the RAM is organized internally as a "**matrix**" with a column address & a row address, e.g., 8 x 512 x 8 bit RAM
  ∴ (8 x 512) x 8 = 4k x 8 RAM, but we use 9 bits as a row address and 3 bits for a column address. (512 = 2^9, 8 = 2^3, 4k = 2^{12})
  Total Storage = 2^{12} words (word=8 bits)
  or 000 0 0000 0000
  to 111 1 1111 1111
  or $000 (=000H) to $FFF (=FFFH)



- We can think of lines A_{11}~A_9 as "**column selector**" and lines A_8~A_0 as a "**row selector**." Each selected element is eight bits deep.
- The user does not really care how the RAM is organized. He only "sees" the fact that it stores 4k x 8.

14


EEL3701
Dynamic RAM (DRAM)
• DRAM is also "volatile" RAM
• DRAM must be periodically rewritten (refreshed) else the info will be lost!
• DRAM's have higher density (more bits per unit area of silicon) and are "faster" (but since we have to refresh them, the "net" time may be slower than SRAM).
• Can get 16M x 8 bits (16M= 4k x 4k = 2^24) and larger.
• For the details of "refreshing" and timing involve using lines RAS & CAS, see next slide.
General DRAM Model
• n-bits for row
• n-bits for column
• => 2*n address bits
Address Bus
n
A n-1 ~ A 0
D m-1 ~ D 0
m
Data Bus
RAS
CAS
WE
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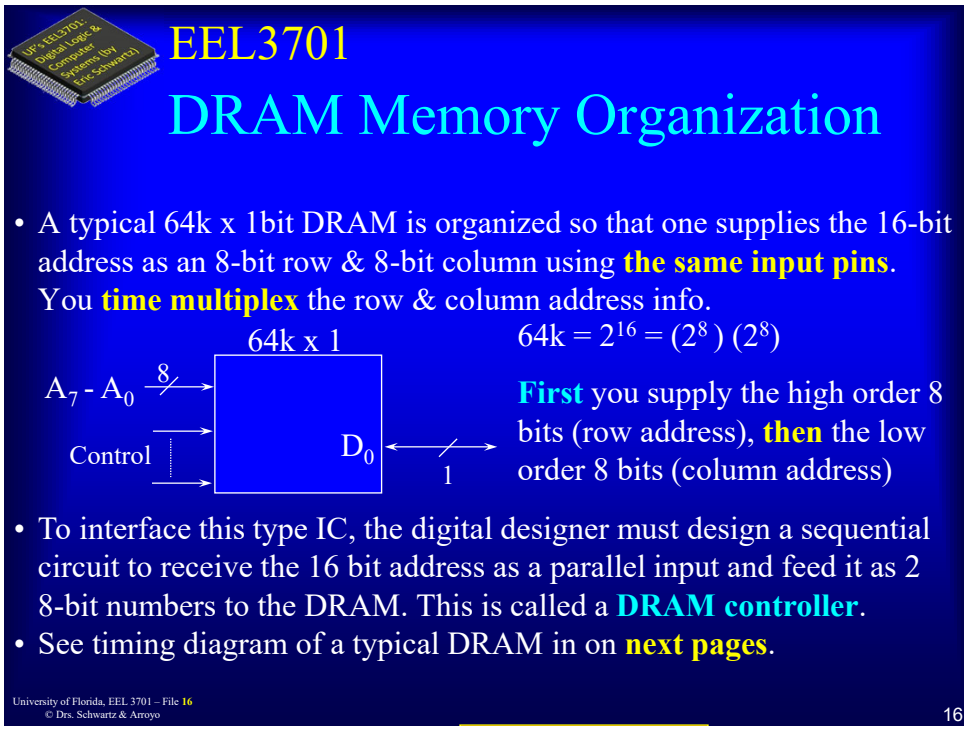
EEL3701
DRAM Memory Organization
• A typical 64k x 1bit DRAM is organized so that one supplies the 16-bit address as an 8-bit row & 8-bit column using the same input pins. You time multiplex the row & column address info.
64k x 1
64k = 2^16 = (2^8) (2^8)
A7 - A0
8
Control
D0
1
First you supply the high order 8 bits (row address), then the low order 8 bits (column address)
• To interface this type IC, the digital designer must design a sequential circuit to receive the 16 bit address as a parallel input and feed it as 2 8-bit numbers to the DRAM. This is called a DRAM controller.
• See timing diagram of a typical DRAM in on next pages.
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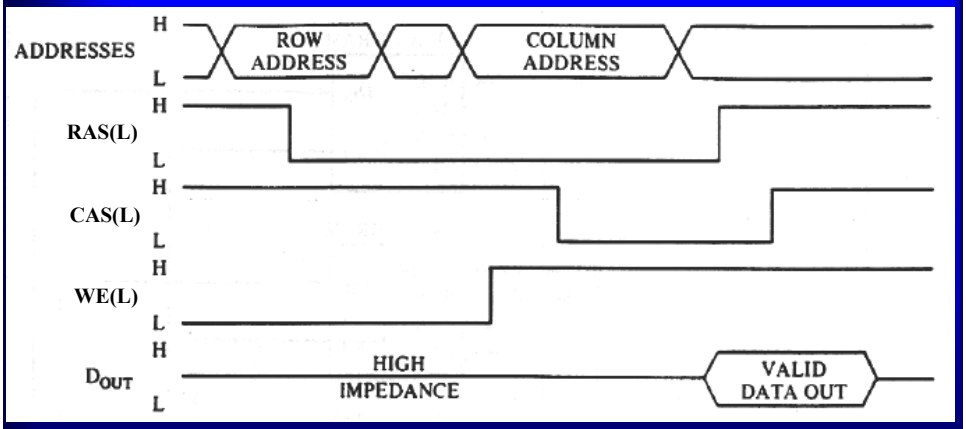
EEL3701

DRAM Read Cycle



Ref Lam Fig 6.31

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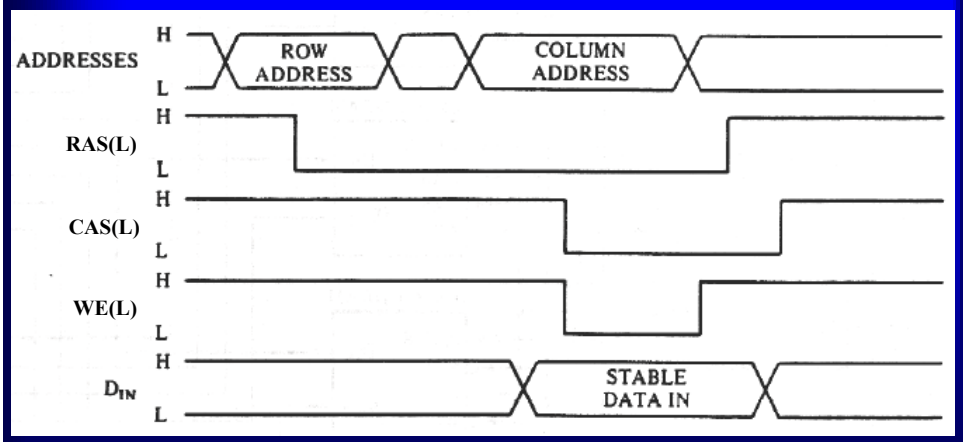
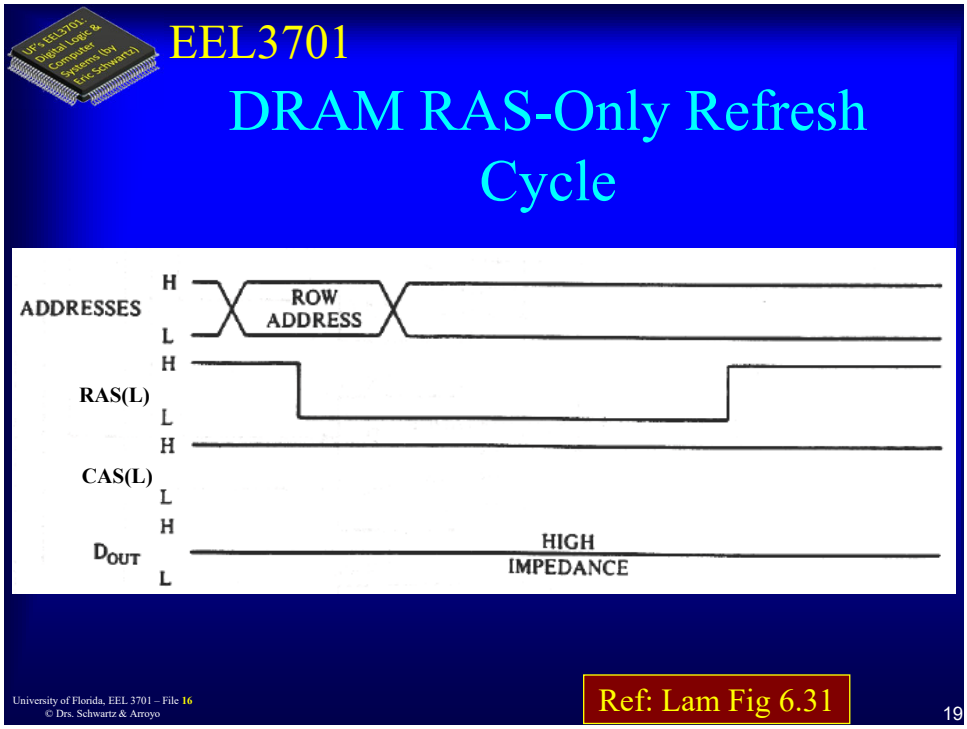
EEL3701

DRAM Write Cycle



Ref: Lam Fig 6.31

18


EEL3701
DRAM RAS-Only Refresh Cycle
ADDRESSES
H
L
ROW ADDRESS
RAS(L)
H
L
CAS(L)
H
L
D_{OUT}
H
L
HIGH IMPEDANCE
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Ref: Lam Fig 6.31
19

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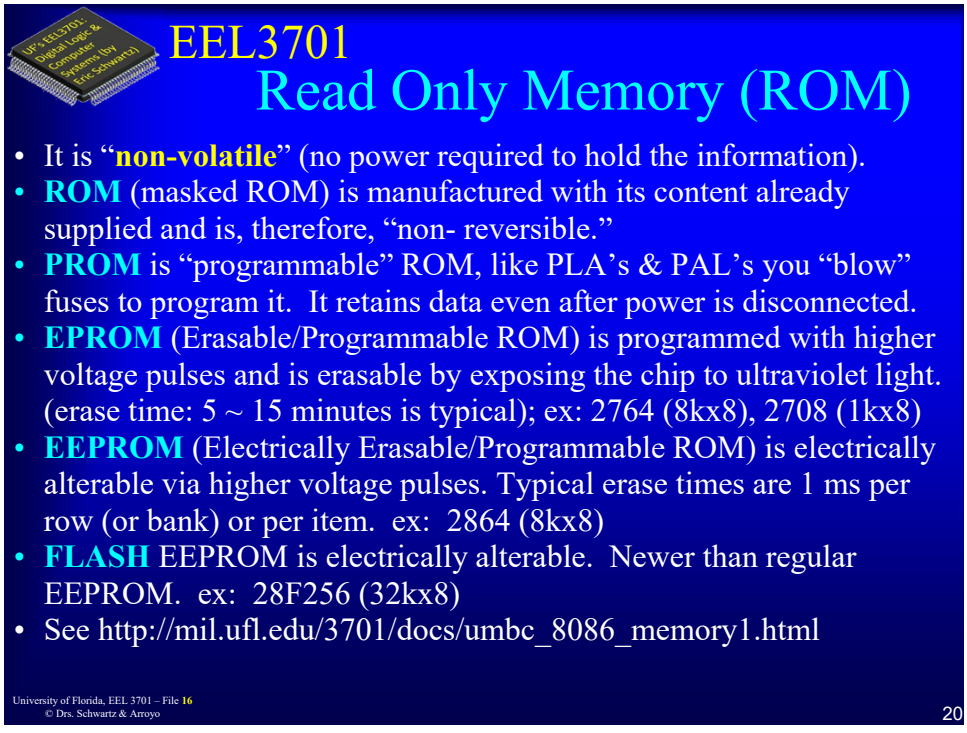
EEL3701
Read Only Memory (ROM)
• It is "non-volatile" (no power required to hold the information).
• ROM (masked ROM) is manufactured with its content already supplied and is, therefore, "non- reversible."
• PROM is "programmable" ROM, like PLA's & PAL's you "blow" fuses to program it. It retains data even after power is disconnected.
• EPROM (Erasable/Programmable ROM) is programmed with higher voltage pulses and is erasable by exposing the chip to ultraviolet light. (erase time: 5 ~ 15 minutes is typical); ex: 2764 (8kx8), 2708 (1kx8)
• EEPROM (Electrically Erasable/Programmable ROM) is electrically alterable via higher voltage pulses. Typical erase times are 1 ms per row (or bank) or per item. ex: 2864 (8kx8)
• FLASH EEPROM is electrically alterable. Newer than regular EEPROM. ex: 28F256 (32kx8)
• See http://mil.ufl.edu/3701/docs/umbc_8086_memory1.html
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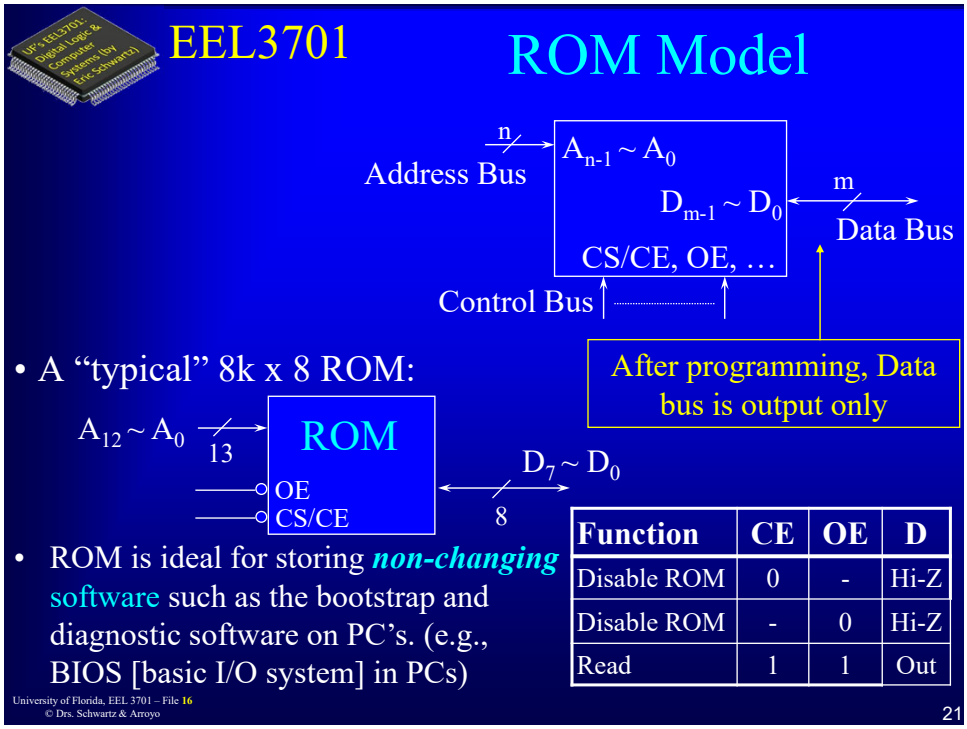

Function	CE	OE	D
Disable ROM	0	-	Hi-Z
Disable ROM	-	0	Hi-Z
Read	1	1	Out

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Operation	CE/PRG	OE	Vpp	D_{7-0}
Read	L	L	+5 V	Out
Standby	H	-	+5 V	High Z
Program	L → H	H	+25 V	In
Program Verify	L	L	+25 V	Out
Program Inhibit	L	H	+25 V	High Z

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EEL3701
Example EEPROM Operation
2864: 8k × 8 EEPROM
2864
EEPROM
13
8
A12-0
D7-0
CE
OE
WE
Vcc
+5V
NC 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
I/O0 11
I/O1 12
I/O2 13
GND 14
28 VCC
27 WE
26 NC
25 A8
24 A9
23 A11
22 OE
21 A10
20 CE
19 I/O7
18 I/O6
17 I/O5
16 I/O4
15 I/O3
Operation | CE | OE | WE | D7-0
Read | L | L | H | Out
Write | L | H | L | In
Standby/Write Inhibit | H | - | - | High Z
Write Inhibit | - | - | H |
Write Inhibit | - | L | - |
Output Disable | - | H | - | High Z
Chip Erase | L | 12V | L | High Z
H = +5V
• I/O7-0 = D7-0 = Data Bus
• A12-0 = A12-0 = Address Bus
• NC = No Connection
See Software/Docs: "2864"
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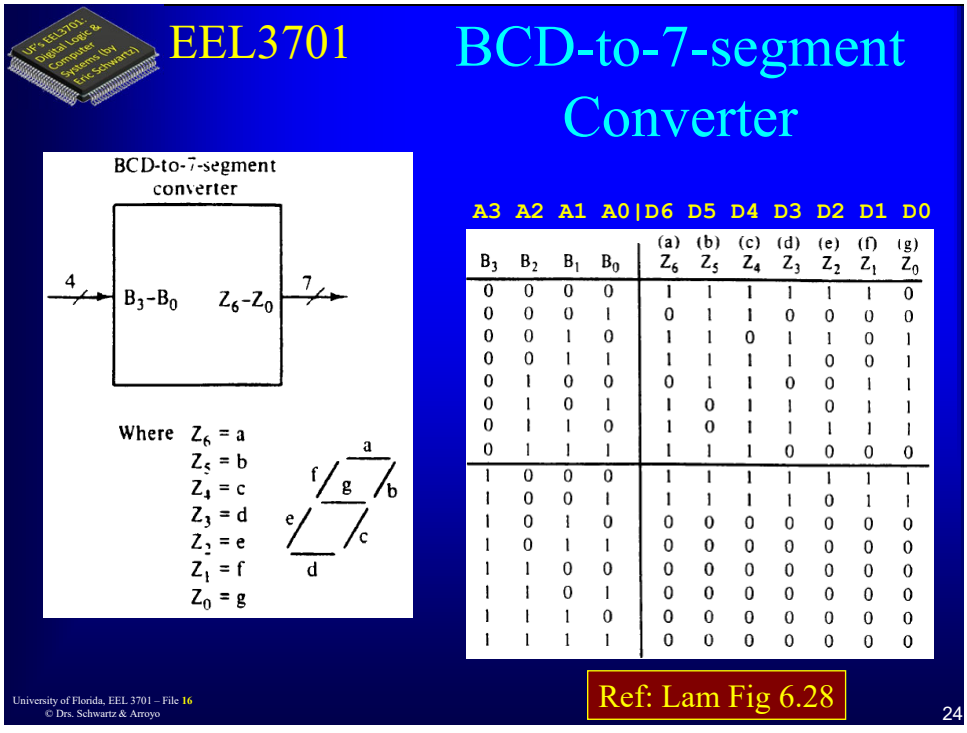
EEL3701
BCD-to-7-segment Converter
BCD-to-7-segment converter
4
B3-B0
Z6-Z0
7
Where Z6 = a
Z5 = b
Z4 = c
Z3 = d
Z2 = e
Z1 = f
Z0 = g
a
f
g
b
e
c
d
A3 A2 A1 A0 | D6 D5 D4 D3 D2 D1 D0
B3 B2 B1 B0 | (a) Z6 (b) Z5 (c) Z4 (d) Z3 (e) Z2 (f) Z1 (g) Z0
0 0 0 0 | 1 1 1 1 1 1 0
0 0 0 1 | 0 1 1 0 0 0 0
0 0 1 0 | 1 1 0 1 1 0 1
0 0 1 1 | 1 1 1 1 0 0 1
0 1 0 0 | 0 1 1 0 0 1 1
0 1 0 1 | 1 0 1 1 0 1 1
0 1 1 0 | 1 0 1 1 1 1 1
0 1 1 1 | 1 1 1 0 0 0 0
1 0 0 0 | 1 1 1 1 1 1 1
1 0 0 1 | 1 1 1 1 0 1 1
1 0 1 0 | 0 0 0 0 0 0 0
1 0 1 1 | 0 0 0 0 0 0 0
1 1 0 0 | 0 0 0 0 0 0 0
1 1 0 1 | 0 0 0 0 0 0 0
1 1 1 0 | 0 0 0 0 0 0 0
1 1 1 1 | 0 0 0 0 0 0 0
Ref: Lam Fig 6.28
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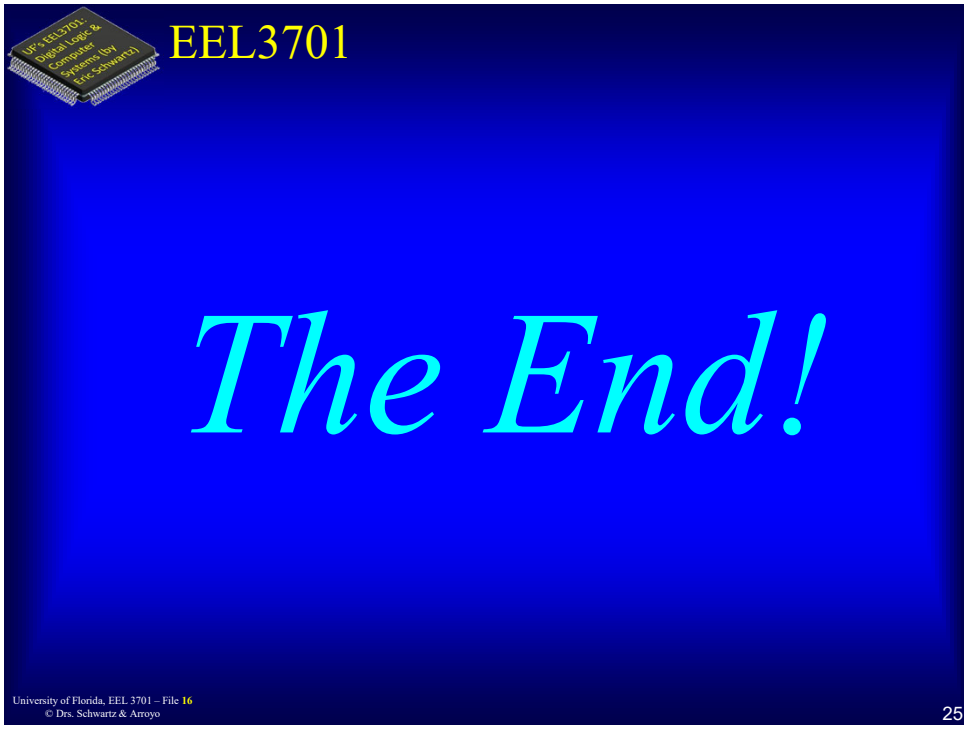
EEL3701
The End!
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